In the Specification

Please delete from line 20, page 3 through line 26, page 4.

On page 10, line 16-17, please delete "Serial No. _____ (Micron Docket No. 97-0675)" and insert --Serial No. 09/141,236, filed August 27, 1998--.

On page 10, line 18-19, please delete "Serial No. _____ (Micron Docket No. 97-0861)" and insert -- Serial No. 09/141,431, filed August 27, 1998--.

In the Claims

Please cancel claims 1-26 according to the Request for Filing a Divisional Application filed herewith. Please amend claim 30 to correct dependancy of the claim. All the pending claims are reproduced herein for the convenience with the amended claim so marked.

27. A semiconductor device structure, the structure comprising:

a substrate assembly including a surface; and

a diffusion barrier layer over at least a portion of the surface, wherein the diffusion barrier layer is formed of $RuSi_x$, where x is in the range of about 0.01 to about 10.

28. The structure of claim 27, wherein x is in the range of about 1 to about 3.

29. The structure of claim 28, wherein x is about 2.0.

30. The structure of claim [27] 23, wherein the at least a portion of the surface is a silicon containing surface and further wherein the structure includes one or more additional conductive layers over the diffusion barrier layer formed of at least one of a metal and a conductive metal oxide.

31. The structure of claim 30, wherein the one or more conductive layers are formed from materials selected from the group of RuO_2, RhO_2, MoO_2, IrO_2, Ru, Rh, Pd, Pt, and Ir.

32. A capacitor structure comprising:

a first electrode;

a high dielectric material on at least a portion of the first electrode; and

a second electrode on the dielectric material, wherein at least one of the first and second electrode comprises a diffusion barrier layer formed of $RuSi_x$, where x is in the range of about 0.01 to about 10.

33. The structure of claim 32, wherein x is in the range of about 1 to about 3.

34. The structure of claim 32, wherein the diffusion barrier layer of the first electrode is formed on at least a portion of a silicon containing region and further wherein the structure includes one or more additional conductive layers over the diffusion barrier layer formed of at least one of a metal and a conductive metal oxide.

35. The structure of claim 34, wherein the one or more additional conductive layers are formed from materials selected from the group of RuO_2, RhO_2, MoO_2, IrO_2, Ru, Pt, and Ir.

36. A integrated circuit structure comprising:

a substrate assembly including at least one active device and a silicon containing region; and

an interconnect formed relative to the at least one active device and the silicon containing region, the interconnect including a diffusion barrier layer on at least a portion of the silicon containing region, wherein the diffusion barrier layer is formed of $RuSi_x$, where x is in the range of about 0.01 to about 10.

37. The structure of claim 36, wherein x is in the range of about 1 to about 3.